O.P.Code: 20EC0417	R20	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year I Semester Regular & Supplementary Examinations February-2024

DIGITAL SIGNAL PROCESSING

(Electronics & Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Explain the steps in Decimation in Time FFT algorithm with necessary diagram.	CO1	L2	6M
	b	Find the linear convolution of the sequences $x(n)$ and $h(n)$ using DFT. $x(n) = \{1,0,2\}$, $h(n) = \{1,1\}$	CO1	L2	6M
		OR			
2		Compute 8-point DFT of the sequence $x(n) = \{0,1,2,3,4,5,6,7\}$using Radix-2 DIF-FFT Algorithm.	CO1	L2	12M

UNIT-II

3		Design a digital Chebyshev IIR filter satisfying the following constraints. Let T=1s, apply Bilinear transformation. $0.707 \leq \lvert H(w)\rvert \leq 1 \quad ; 0 \leq w \leq 0.2\pi$ $\lvert H(w)\rvert \leq 0.1 \quad ; 0.5\pi \leq w \leq \pi$	CO2	L3	12M
		OR			
4	a	How a digital filter is designed? List the methods for converting analog filter TF to digital filter TF.	CO2	L3	6M
	b	Explain the steps in the design of an analog Butterworth low pass filter.	CO2	L3	6M

UNIT-III

5	a	Write the design steps of FIR filter using Frequency sampling technique.	CO2	L2	6M
	b	Give the equations for Rectangular, Hanning and Hamming window and explain its significance.	CO2	L2	6M
		OR			
6		Design a filter with following data, using a Hamming window with N=7. $H_d(e^{jw}) = 1 \; for \; -\frac{\pi}{4} \leq w \leq \frac{\pi}{4}$ $= 0 \qquad \frac{\pi}{4} \leq \lvert w\rvert \leq \pi$	CO3	L3	12M

UNIT-IV

7		Find the steady state variance of the noise in the output due to quantization of input for the first order filter. $y(n) = a\,y(n-1) + x(n)$.	CO5	L3	12M
		OR			
8	a	Discuss briefly about different types of number representation with examples.	CO5	L2	6M
	b	Compare fixed point and floating point arithmetic.	CO5	L4	6M

UNIT-V

9		Explain different applications of PDSPs in detail.	CO6	L2	12M
		OR			
10	a	Draw and explain Arithmetic and logical unit (ALU) of TMS320C54x	CO6	L2	6M
	b	Explain internal memory organization in TMS320C54x architecture.	CO6	L2	6M

***** END *****